CLAIMS

1. A gain switching circuit that switches a conversion gain of a preamplifier, the preamplifier outputting a voltage signal by amplifying an output current of a photo-detecting element that converts a burst optical signal into an electrical signal, the preamplifier being configured with a series circuit formed with a first resistor and a first switching element and a series circuit formed with a second resistor and a second switching element respectively connected in parallel with a feedback resistor, the gain switching circuit inputting a first gain switching period for switching to a first conversion gain and a second gain switching period for switching to a second conversion gain from outside upon receiving an output from the preamplifier, the gain switching circuit comprising:

a first operating unit that generates a first switching element operating signal for closing the first switching element within the first gain switching period; and

a second operating unit that generates a second switching element operating signal for closing the second switching element within the second gain switching period.

2. The gain switching circuit according to claim 1, wherein

the first gain switching period is different from the second gain switching period.

3. The gain switching circuit according to claim 1, wherein

closing of the second switching element by the second operating unit within the second gain switching period is enabled after the first switching element is closed by the

first operating unit within the first gain switching period.

4. The gain switching circuit according to claim 1, wherein

the first operating unit outputs the first switching element operating signal, when an output level of the preamplifier exceeds a first discrimination level, if a timing when the output level exceeds the first discrimination level exceeds is within the first gain switching period, and

the second operating unit outputs the second switching element operating signal, when the output level of the preamplifier exceeds a second discrimination level, if the first switching element operating signal has been output, and if a timing when the output level exceeds the second discrimination level is within the second gain switching period.

5. The gain switching circuit according to claim 4, wherein

following relation is satisfied

$V1<kV2$

where V1 is the first discrimination level, V2 is the second discrimination level is V2, and k is an amount of lowering a gain of the preamplifier when the first switching element is closed based on the first discrimination level.

6. A gain switching circuit that switches a conversion gain of a preamplifier, the preamplifier outputting a voltage signal by amplifying an output current of a photo-detecting element that converts a burst optical signal into an electrical signal, the preamplifier being configured

with a series circuit formed with a first resistor and a first switching element and a series circuit formed with a second resistor and a second switching element respectively connected in parallel with a feedback resistor, the gain switching circuit comprising:

a gate generating circuit that generates, upon receiving an output of the preamplifier, a gate signal for switching to a predetermined conversion gain within a gain switching period;

a first operating unit that generates a first switching element operating signal for closing a first switching element within the gain switching period; and

a second operating unit that generates a second switching element operating signal for closing a second switching element within the gain switching period.

7. The gain switching circuit according to claim 6, wherein

closing of the second switching element by the second operating unit is enabled after the first switching element is closed by the first operating unit within the gain switching period.

8. The gain switching circuit according to claim 7, wherein

when the first switching element operating signal is generated using a first discrimination level and the second switching element operating signal is generated using a second discrimination level, the gate generating circuit generates the gate signal based on a third discrimination level that satisfies

$V10<V1$ and $V10<V2$

where V1 is the first discrimination level, V2 is the econd

discrimination level, and V10 is the third discrimination level.

9. The gain switching circuit according to claim 8, wherein

the gate generating circuit includes a counter circuit that generates a clock signal, and

the gate generating circuit generates a gate signal having a time width of a predetermined number of clocks by using the clock signal generated by the counter circuit.

10. The gain switching circuit according to claim 7, wherein

when the first switching element operating signal is generated using a first discrimination level and the second switching element operating signal is generated using a second discrimination level, the gate generating circuit generates the gate signal based on a third discrimination level and a fourth discrimination level that satisfy

$V10<V11<V1$ and $V10<V11<V2$

where V1 is the first discrimination level, V2 is the second discrimination level, V10 is the third discrimination level, and V11 is the fourth discrimination level.

11. The gain switching circuit according to claim 10, wherein

the gate generating circuit includes

a first variation-point detecting circuit that detects a variation point of a signal that is detected at the third discrimination level; and

a second variation-point detecting circuit that detects a variation point of a signal that is detected at

the fourth discrimination level, and

the gate generating circuit generates a logical product signal of a first basic gate signal that is generated by the first variation-point detecting circuit with a time width of a predetermined variation point count length and a second basic gate signal that is generated by the second variation-point detecting circuit with a time width of a predetermined variation point count length as the gate signal.